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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,830	12/03/2001	Taiyuu Miyamoto	027260-504	7164

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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/998,830	MIYAMOTO, TAIYUU	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2 and 8-9 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 6/30/2008.

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/30/2008 has been entered.

Withdrawn objections and rejections

4. The 112 first paragraph written description rejections for claims 5-6 are withdrawn due to cancellation of the claims.

Maintained Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1-2 and 8-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1 recites "a first mode, wherein the central processing unit fetches instruction from an external memory, and a second mode, wherein the central processing unit fetches instructions from the internal memory and inhibits fetching instructions from the external memory." Applicant cited page 7 paragraph 3 and page 8 paragraph 2 for support. These paragraphs generally support most of the claimed limitations, supporting a first mode fetching from external memory and a second mode fetching from internal memory. However, these paragraphs from the specification do not support the second mode inhibiting fetching instructions from the external memory. Thus, the examiner has found no support of the claimed limitation to show one of ordinary skill in the art that the limitation had possession of the claimed invention at the time the application was filed.

7. Claims 2 and 8-9 are rejected due to their dependency.

New Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-2 and 8-9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sibigtroth et al. (U.S. 5,432,950).

10. As per claim 1:

Sibigtroth disclosed a microcomputer comprising an internal memory (Sibigtroth: Figure 1 elements 13 and 20)(These elements are the internal memory of the data processing system.), a central processing unit (Sibigtroth: Figure 1 element 14), and a functional block comprising a peripheral block (Sibigtroth: Figure 1 element 12), built-in said microcomputer, wherein said internal memory has first program memory (Sibigtroth: Figure 1 element 20, column 4 lines 61-67 continued to column 5 lines 1-6) and a reprogrammable nonvolatile memory including a first area storing program codes and a second area storing user data (Sibigtroth: Figure 1 elements 13 and 24, column 3 lines 9-20)(Element 13 is a memory that can be a plurality of different types of memories, including reprogrammable nonvolatile memory. Thus, it's obvious to one of ordinary skill in the art that element 13 is an EEPROM. The memory stores data and instructions.), and in which a lock code is written in a specified area (Sibigtroth: Figure 1 element 20, column 4 lines 61-67 continued to column 5 lines 1-6)(The enable signal is stored within element 20.); and

the microcomputer has a first mode, wherein the central processing unit fetches instruction from an external memory, and a second mode, wherein the central processing unit fetches instructions from the internal memory and inhibits fetching instructions from the external memory (Sibigtroth: Figure 1 elements 18, 22, and 24, column 4 lines 15-39 and column 9 lines 36-65)(The second mode is the secure mode and the first mode is the non-secure mode. The second secure mode prohibits fetching instructions from external memory. Figure 1 shows that the processor normally fetches

instructions and data via an address bus to the internal and external memories. Therefore, the non-secure mode is capable of fetching instructions from internal and external memory. The secure mode is limited to fetching instructions from internal memory.), and comprising:

a first decoding circuit connected with said nonvolatile memory, which reads out said lock code, and decodes said lock code (Sibigtroth: Figure 2 element 50)(The inverter reads out the enable signal and decodes it.);

a logic circuit that performs a predetermined operation on an externally input mode bit, by the output from the first decoding circuit (Sibigtroth: Figure 2 element 52)(The AND gate takes in the decoded enable bit and the instruction fetch bit, which is external to all circuits shown in figure 1, including the instruction inhibit unit.); and

a second decoding circuit that decodes the processed mode bit by receiving the output from said logic circuit, and sends the obtained results to said functional block (Sibigtroth: Figure 2 element 54)(The OR circuit is the second decoding circuit, which decodes the bit output from the AND circuit, and sends its output to the functional block.), wherein

when a first value is set into the specified area as the lock code, the microcomputer is configured to be set into the second mode (Sibigtroth: Figure 1 element 18, column 9 lines 36-65)(The enable signal indicates the data processing system is in a secure mode. The secure mode inhibits fetching instructions from external memory.), and

when a second value is set into said specified area as the lock code, the central processing unit fetches instructions from the first area of the reprogrammable nonvolatile memory instead of the first program memory by the reprogrammable nonvolatile memory allocating on the address area to be allocated to the first program memory (Sibigtroth: Figure 1 elements 18, 22, and 24, column 4 lines 15-39 and column 9 lines 36-65)(The second mode is the secure mode and it prohibits fetching instructions from external memory. Figure 1 shows that the processor normally fetches instructions and data via an address bus to the internal memory element 13. Thus, the secure mode fetches instructions from the EEPROM element 13 instead of element 20.).

11. As per claim 2:

Sibigtroth and Phillips disclosed the microcomputer of claim 1, wherein said logic circuit consists of an AND circuit (Sibigtroth: Figure 2 element 52).

12. As per claim 8:

Sibigtroth disclosed the microcomputer of claim 1, wherein said reprogrammable nonvolatile memory consists of a data memory and a program memory (Sibigtroth: Figure 1 elements 13 and 24, column 3 lines 9-20)(Element 13 is a memory that can be a plurality of different types of memories, including reprogrammable nonvolatile memory. Thus, it's obvious to one of ordinary skill in the art that element 13 is an EEPROM. The memory stores data and instructions.).

13. As per claim 9:

Sibigtroth disclosed the microcomputer of claim 1, wherein the logic circuit masks the input mode bit by the decoded lock code (Sibigtroth: Figure 2 element 52)(The selector circuit (And gate 52) takes decoded enable bit and Instruction Fetch bit, and based on the output of the AND gate 52, the external terminal (shown in figure 2) performs different functions, i.e., either allowing the bus 30 to connect to the Data bus 24 or not allowing. The AND circuit provides the mask.).

Response to Arguments

14. The arguments presented by Applicant in the response, received on 6/30/2008 are not considered persuasive.

15. Applicant argues "Sibigtroth does not teach or suggest when a second value is set into said specified area as the lock code, the central processing unit fetches instructions from the first area of the reprogrammable nonvolatile memory instead of the first program memory by the reprogrammable nonvolatile memory allocating on the address area to be allocated to the first program memory."

This argument is not found to be persuasive for the following reason. The second mode is the secure mode and it prohibits fetching instructions from external memory. Figure 1 shows that the processor normally fetches instructions and data via an address bus to the internal memory element 13. Thus, the secure mode fetches instructions from the EEPROM element 13 instead of element 20.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Jacob Petranek
Examiner, Art Unit 2183